What is claimed is:

1. A device in a process, the device comprising:

a substrate;

a device structure formed over the substrate; and

a masking structure formed over the device structure, the masking structure including an amorphous carbon layer, wherein the amorphous carbon layer is transparent in visible light range.

2. The device of claim 1, wherein the amorphous carbon layer has an absorption coefficient between about 0.15 and about 0.001 at wavelength of 633 nanometers.

3. The device of claim 1, wherein the visible light range includes electromagnetic radiation having wavelengths between 400 nanometers and 700 nanometers.

4. The device of claim 1, wherein the amorphous carbon layer has a thickness greater than 4000 Angstroms.

5. The device of claim 4, wherein the device structure has a thickness greater than 40000 Angstroms.

6. The device of claim 1, wherein the masking structure further includes a silicon oxynitride layer formed over the amorphous carbon layer.

7. The device of claim 1, wherein the masking structure further includes a photoresist layer.

8. The device of claim 7, wherein the masking structure further includes an antireflective layer.

9. The device of claim 7 wherein the photoresist layer includes at least one opening.

10. The device of claim 9, wherein the amorphous carbon layer includes at least one opening continuous with the at least one opening of the photoresist layer.

11. The device of claim 1, wherein the device structure includes a layer selected from a material in a group consisting of a conducting material, a non-conducting material, and a semiconducting material.

12. The device of claim 11, wherein the device structure further includes an amorphous carbon layer, wherein the amorphous carbon layer of the device structure is transparent in visible light range.

13. A mask structure for a device, the mask structure comprising:

an amorphous carbon layer, wherein the amorphous carbon layer is transparent to radiation having wavelengths between 400 nanometers and 700 nanometers.

14. The mask structure of claim 13, wherein the amorphous carbon layer has an absorption coefficient between about 0.15 and about 0.001 at wavelength of 633 nanometers.

15. The mask structure of claim 13, wherein the amorphous carbon layer has a thickness of at least 4000 Angstroms.

16. The mask structure of claim 13 further comprising a photoresist layer.

17. The mask structure of claim 16 further comprising a cap layer formed over the amorphous carbon layer.

18. The mask structure of claim 17, wherein the a cap layer includes silicon oxynitride.

19. The mask structure of claim 16, wherein the photoresist layer includes at least one opening.

20. The mask structure of claim 19, wherein the amorphous carbon layer includes at least one opening continuous with the at least one opening of the photoresist layer.

21. A memory device in a process, the memory device comprising:

a substrate having a plurality of doped regions;

device structure formed over the substrate, the device structure including a plurality of gate structures, a plurality of contacts, each of the contacts being located between two gate structure and contacting one of the doped regions, and an insulating layer formed over the gate structures and the contacts; and

a masking structure formed over the device structure, the masking structure including an amorphous carbon layer, wherein the amorphous carbon layer is transparent in visible light range.

22. The memory device of claim 21, wherein the amorphous carbon layer has a thickness of at least 4000 Angstroms.

23. The memory device of claim 22, wherein the device structure has a thickness of at least 40000 Angstroms.

24. The memory device of claim 21, wherein the masking structure further includes a silicon oxynitride layer formed over the amorphous carbon layer.

25. The memory device of claim 21, wherein the masking structure further includes a photoresist layer.

26. The memory device of claim 25, wherein the masking structure further includes an antireflective layer.

27. The memory device of claim 25, wherein the photoresist layer includes at least one opening of the photoresist layer.

28. The memory device of claim 27, wherein the amorphous carbon layer includes at least one opening continuous with the at least one opening of the photoresist layer.

29. The memory device of claim 28, wherein the insulating layer includes at least one opening continuous with both of the at least one opening of the amorphous carbon layer and the at least one opening of the photoresist layer.

30. The memory device of claim 21, wherein the device structure further includes a barrier layer located between the gate structures and the contacts.

31. The memory device of claim 21, wherein the amorphous carbon layer has an absorption coefficient between about 0.15 and about 0.001 at wavelength of 633 nanometers.

32. A system comprising:

a chamber having a temperature between about 200°C and about 500°C; and

a wafer place in the chamber, the wafer including a die, the die including a substrate, a device structure formed over the substrate, and a masking structure formed over the device structure, the masking structure including an amorphous carbon layer, wherein the amorphous carbon layer is transparent in visible light range.

33. The system of claim 32, wherein the amorphous carbon layer has a thickness greater than 4000 Angstroms.

34. The system of claim 33, wherein the device structure has a thickness greater than 40000 Angstroms.

35. The system of claim 34, wherein the masking structure further includes a silicon oxynitride layer formed over the amorphous carbon layer.

36. The system of claim 32, wherein the masking structure further includes a photoresist layer.

37. The system of claim 36, wherein the masking structure further includes an antireflective layer.

38. The system of claim 36, wherein the photoresist layer includes at least one opening.

39. The system of claim 38, wherein the amorphous carbon layer includes at least one opening continuous with the at least one opening of the photoresist layer.

40. The system of claim 32, wherein the device structure includes a conductive layer.

41. The system of claim 40, wherein the device structure further includes an insulating layer.

42. The system of claim 41, wherein the device structure further includes an antireflective layer.

43. The system of claim 42, wherein the device structure further includes an amorphous carbon layer.

44. The system of claim 43, wherein the masking structure further includes a photoresist layer.

45. The system of claim 44, wherein the masking structure further includes an antireflective layer.

46. The system of claim 32, wherein the at least one die includes circuitry for a memory device.

47. The system of claim 32, wherein the at least one die includes circuitry for a processor.

48. The system of claim 32, wherein the chamber is a plasma enhanced vapor chemical deposition chamber.

49. A method comprising:

forming a device structure over a substrate; and

forming a masking structure over the substrate including forming an amorphous carbon layer, wherein the amorphous carbon layer is transparent in visible light range.

50. The method of claim 49, wherein forming an amorphous carbon layer includes forming the amorphous carbon layer having a thickness of at least 4000 Angstroms.

51. The method of claim 50, wherein forming the device structure including forming the device structure having a thickness of at least 40000 Angstroms.

52. The method of claim 49, wherein forming the masking structure further includes forming a silicon oxynitride layer over the amorphous carbon layer.

53. The method of claim 52, wherein the silicon oxynitride layer is in situ deposited together with the amorphous carbon layer.

54. The method of claim 49, wherein forming an amorphous carbon layer includes patterning the amorphous carbon layer to form a patterned amorphous carbon layer.

55. The method of claim 54, wherein forming a device structure includes patterning the device structure using the patterned amorphous carbon layer as a mask.

56. The method of claim 49, wherein forming a masking structure further includes forming a patterned photoresist layer.

57. The method of claim 56, wherein forming a masking structure further includes patterning the amorphous carbon layer using the patterned photoresist layer as a mask.

58. The method of claim 56, wherein forming a device structure includes patterning the device structure using the patterned amorphous carbon layer as a mask.

59. The method of claim 49, wherein the amorphous carbon layer has an absorption coefficient between about 0.15 and about 0.001 at wavelength of 633 nanometers.

60. The method of claim 59, wherein the amorphous carbon is formed at a temperature range of about 200°C to about 500°C.

61. The method of claim 49, wherein the visible light range includes electromagnetic radiation having wavelengths between 400 nanometers and 700 nanometers.

62. A method comprising:

forming a device structure over a substrate; and

forming a masking structure over the device structure including forming an amorphous carbon layer at a temperature range of about 200°C to about 500°C.

63. The method of claim 62, wherein forming the masking structure further includes forming a silicon oxynitride layer over the amorphous carbon layer.

64. The method of claim 63, wherein the silicon oxynitride layer is in situ deposited together with the amorphous carbon layer.

65. The method of claim 64, wherein the amorphous carbon layer has an absorption coefficient between about 0.15 and about 0.001 at wavelength of 633 nanometers.

66. The method of claim 62, wherein forming an amorphous carbon layer includes forming the amorphous carbon layer at a temperature from about 200°C to about below 300°C.

67. The method of claim 62, wherein forming an amorphous carbon layer includes forming the amorphous carbon layer having a thickness greater than 4000 Angstroms.

68. The method of claim 67, wherein forming the device structure includes forming the device structure having a thickness greater than 40000 Angstroms.

69. The method of claim 62, wherein forming an amorphous carbon layer is performed in a chamber subjected to a pressure range of about 4 Torr to about 6.5 Torr, a radio frequency power range of about 450 Watts to about 1000 Watts, and a gas mixture including propylene.

70. The method of claim 69, wherein the gas mixture further includes helium.

71. The method of claim 70, wherein the propylene is introduced into the chamber at a flow rate of between 500 standard cubic centimeters per minute (sccm) and 4000 sccm.

72. The method of claim 71, wherein the helium is introduced into the chamber at a flow rate of between 250 sccm and 1000 sccm.

73. A method comprising:

forming a device structure on a substrate;

forming a making structure over the device structure including forming an amorphous carbon layer, wherein the amorphous carbon layer is transparent in visible light range; and

etching the device structure using the amorphous carbon layer as a mask.

74. The method of claim 73, wherein forming an amorphous carbon layer is performed in a chamber with a temperature range of about 200°C to about 500°C, a pressure range of about 4 Torr to about 6.5 Torr, a radio frequency power range of about 450 Watts to about 1000 Watts, and a mixture of gas including propylene.

75. The method of claim 74, wherein the propylene is introduced into the chamber at a flow rate between 500 standard cubic centimeters per minute (sccm) and 4000 sccm.

76. The method of claim 75, wherein the helium is introduced into the chamber at a flow rate between 250 sccm and 1000 sccm.

77. The method of claim 73, wherein forming an amorphous carbon layer is performed by a chemical vapor deposition process.

78. The method of claim 73, wherein forming the masking structure further includes forming a silicon oxynitride layer over the amorphous carbon layer.

79. The method of claim 78, wherein the silicon oxynitride layer is in situ deposited together with the amorphous carbon layer.

80. The method of claim 79, wherein the amorphous carbon layer has an absorption coefficient between about 0.15 and about 0.001 at wavelength of 633 nanometers.

81. A method comprising:

forming an amorphous carbon layer in which the amorphous carbon layer is transparent in visible light range, wherein forming an amorphous carbon layer is

performed in a chamber with a temperature above 200°C and below 500°C, a pressure range of about 4 Torr to about 6.5 Torr, an radio frequency power range of about 450 Watts to about 1000 Watts, and a mixture of gas including propylene.

82. The method of claim 81, wherein forming an amorphous carbon layer includes forming the amorphous carbon layer having a thickness greater than 4000 Angstroms.

83. The method of claim 81, wherein the mixture of gas further includes helium.

84. The method of claim 83, wherein the propylene is introduced into the chamber at a flow rate of between 500 standard cubic centimeters per minute (sccm) and 4000 sccm.

85. The method of claim 84, wherein the helium is introduced into the chamber at a flow rate of between 250 sccm and 1000 sccm.

86. A method comprising:

forming device structure having a gate structure on a substrate;

forming an amorphous carbon layer over the device structure, wherein the an amorphous carbon layer is transparent in visible light range;

patterning the amorphous carbon layer to form a patterned amorphous carbon layer;

etching the device structure using the patterned amorphous carbon layer as a mask to form a structure of a capacitor of a memory cell; and

removing the patterned amorphous carbon layer.

87. The method of claim 86, wherein patterning the amorphous carbon layer includes:

forming a patterned photoresist layer over the amorphous carbon layer; and

etching the amorphous carbon layer using the patterned photoresist layer as a mask.

88. The method of claim 87 further comprising:

forming a silicon oxynitride layer over the over the amorphous carbon layer before forming the patterned photoresist layer.

89. The method of claim 88, wherein the silicon oxynitride layer is in situ deposited together with the amorphous carbon layer.

90. The method of claim 86, wherein removing the patterned amorphous carbon is performed using an oxygen plasma process.

91. The method of claim 86, wherein removing the patterned amorphous carbon is performed using an oxygen plasma process with one of CF_4 and H_2.

92. A method comprising:

placing a wafer in a chamber, the wafer including at least one die having a substrate and a device structure formed over the substrate;

setting a temperature in the chamber between about 200°C and about 500°C; and

forming a masking structure over the device structure including forming an amorphous carbon layer.

93. The method of claim 92, wherein forming the masking structure further includes forming a silicon oxynitride layer over the amorphous carbon layer.

94. The method of claim 93, wherein the silicon oxynitride layer is in situ deposited together with the amorphous carbon layer.

95. The method of claim 94, wherein the amorphous carbon layer has an absorption coefficient between about 0.15 and about 0.001 at wavelength of 633 nanometers.

96. The method of claim 92, wherein forming an amorphous carbon layer is performed until the amorphous carbon layer has a thickness of at least 4000 Angstroms.

97. The method of claim 92 further comprising:

introducing a propylene into the chamber;

setting a pressure in the chamber between about 4 Torr and about 6.5 Torr; and

subjecting the wafer to a power between about 450 Watts and about 1000 Watts.

98. The method of claim 92 further comprising:

introducing helium into the chamber.

99. The method of claim 98, wherein the propylene is introduced into the chamber at a flow rate between 500 standard cubic centimeters per minute (sccm) and 4000 sccm.

100. The method of claim 99, wherein the helium introduced into the chamber at a flow rate between 250 sccm and 1000 sccm.

101. The method of claim 92, wherein the chamber is a plasma enhanced vapor chemical deposition chamber.

102. A method comprising:

forming a number of memory cells including forming an amorphous carbon layer, wherein the amorphous carbon layer is transparent in visible light range.

103. The method of claim 102, wherein forming a number of memory cells further includes forming a silicon oxynitride layer over the amorphous carbon layer.

104. The method of claim 103, wherein the silicon oxynitride layer is in situ deposited together with the amorphous carbon layer.

105. The method of claim 104, wherein the amorphous carbon layer has an absorption coefficient between about 0.15 and about 0.001 at wavelength of 633 nanometers.

106. The method of claim 102, wherein amorphous carbon layer a thickness of at least 4000 Angstroms.

107. The method of claim 102, wherein forming a number of memory cells includes:

forming a number of transistors; and

forming a number of capacitors having a capacitor plate.

108. The method of claim 107, wherein the capacitor plate is formed after using the amorphous carbon layer to etch an insulating layer over gate structures of the transistors.

109. The method of claim 108, wherein the layer is performed in a chamber with a temperature range of about 200°C to about 500°C, a pressure range of about 4 Torr to about 6.5 Torr, an radio frequency power range of about 450 Watts to about 1000 Watts, and a mixture of gas including propylene.

110. The method of claim 109, wherein the mixture of gas further includes helium.

111. The method of claim 110, wherein the propylene is introduced into the chamber at a flow rate between 500 standard cubic centimeters per minute (sccm) and 4000 sccm.

112 The method of claim 112, wherein the helium is introduced into the chamber at a flow rate between 250 sccm and 1000 sccm.